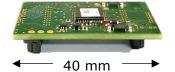


# **4 channel Programmable Delay Module**

#### **Features**

- Four independent delay channel
- Programmable delay in 0.5 ps increments
- 7 ns delay range
- <3 ps input to output RMS jitter</li>
- Up to 50 MHz channel rate
- LVPECL / CML / LVDS channel input
- LVPECL channel output with MUX mode
- Delay control via SPI link
- Operate from DC +5 V
- Compact module: 40 X 25 mm
- Option: Evaluation board with TTL outputs and USB control.



### **Applications**

- Components Test
- OEM Application

- Data de-skewing
- Timing adjustment

### **Description**

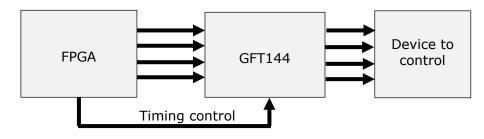
The GFT144 module is a Four Channel Programmable Delay module designed for component test, data de-skewing and timing adjustment. This compact module is well suited for OEM application with an interface via 2 standard connectors, a small size and only one power source.

The core of the module is made with a component (QFN 56 pins) specially designed by Greenfield Technology.

The required delay is accomplished by programming each delay channel via Serial Data Interface. The delay as an increment resolution of typical 0.5 ps in the programmable delay range of 7 ns per channel.

The channel input can be driven directly by differential LVPECL / CML or LVDS logic levels. The output is compatible with DC or AC LVPECL.

**Typical GFT144 application** (see below) would be to control from FPGA application the four timing of a device with high rate and very high resolution.



Typical application



# **4 channel Programmable Delay Module**

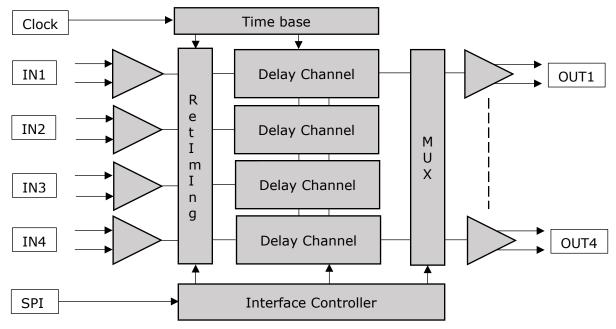
# **Specifications**

| Delay Channel             |   |  |
|---------------------------|---|--|
| Number                    | 4   |  |
| Range                     | 7 ns @ 150 MHz (or 5ns @ 200 MHz) clock input   |  |
| Resolution                | 0.5 ps typical  |  |
| Linearity                 | ±50 ps maximum (without correction)   |  |
| Jitter RMS                | 3 ps (input to output)  |  |
| Channel Input             |   |  |
| Level                     | LVPECL / CML / LVDS   |  |
| Minimum width             | 10 ns   |  |
| Maximum width             | Up to 1 s   |  |
| Connector                 | Samtec  |  |
| Channel Output            |   |  |
| Level                     | LVPECL  |  |
| Rate                      | DC to 50 MHz  |  |
| External Load             | 50/50 $\Omega$ and 50 $\Omega$ (see page 3)   |  |
| Rise Time                 | 750 ps  |  |
| Fall Time                 | 750 ps  |  |
| Insertion Delay           | <5ns (input to output)  |  |
| Mux mode                  | 1 to other channel outputs  |  |
| Connector                 | Samtec  |  |
| Clock input               |   |  |
| Level                     | LVPECL  |  |
| Frequency                 | 150 MHz to 200 MHz  |  |
| General specifications    |   |  |
| Control                   | SPI, Serial data interface  |  |
| Size                      | 40.0 x 25.0 x 10.0 mm   |  |
| Power V/A                 | +5 V / 200mA max.   |  |
| Power connector           | Samtec  |  |
| Option : Evaluation board |   |  |
| Outputs                   | TTL level (adjustable 1.5 to 5 V under 50 $\Omega$ )  |  |
| Trigger mode              | Internal (from programmable timers) or external   |  |
| Interface control         | USB to UART   |  |
| Software tool             | The board is supplied with window software application which include a front panel graphical interface. |  |
| Power Adapter             | External AC (90 -240V) to DC (+ 5V) adapter furnished   |  |



# **4 channel Programmable Delay Module**

#### **Functional overview**



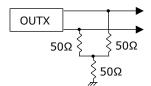
Block diagram

<u>Time base</u>: This function provides time base from external reference (Clock) to synchronize all the functions.

**<u>Retiming</u>**: Allows to synchronize all the "IN" input signal with clock. This function can be inhibited.

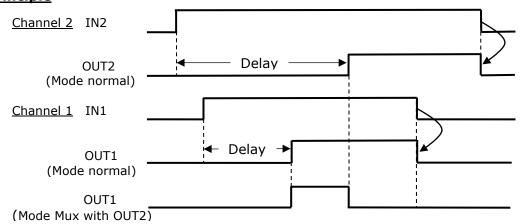
**Delay Channel:** They are 4 independent delay channels. The delay is programmable in 0.5 ps increment. With **Mux** function each delayed output can be AND' to other inverted outputs.

**Channel Output:** Level of the output is LVPECL and must be loaded as showing below.



<u>Interface Controller:</u> it manages internal functions and user interface. All the parameters can be controlled via SPI (serial data interface).

#### **Timing principle**



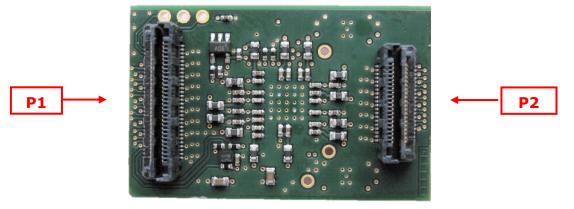


# **4 channel Programmable Delay Module**

## **Top and Bottom view and connectors**



Top view (size x2)



Bottom view (size x2)

#### **Connectors and indicators**

| REF | Description   |
|-----|---|
| P1  | Channel Inputs, Clock, SPI interface: Samtec 2 X 20 pin connector |
| P2  | Channel Outputs, +5V power: Samtec 2 x 10 pin connector           |

# **Ordering information**

| Part number | Description                                      |
|-------------|--|
| GFT144      | 4 channel programmable Delay Module Base version |
| GFT144-01   | GFT144 with evaluation board                     |